

# Molecular Foundry Example Proposal #1

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## Vapor Transport Deposition for III-V Thin Film Photovoltaics

### Foundry Facilities

Facility	Description
<b>Imaging/Manipulation:</b> (lead)	Will work closely with Dr. Shaul Aloni to study and improve the GaAs materials synthesis (at [REDACTED]) and characterization at the foundry. We will use two-photon photoluminescence microscopy along with TEM imaging to make defects and spatially dependent materials properties in the GaAs materials synthesized.
<b>Fabrication:</b> (support)	We require the use of nanoimprint lithography to pattern Si growth substrates for selective area epitaxy.
<b>Inorganic:</b> (support)	We will work closely with Dr. Shaul Aloni to study and improve the GaAs materials synthesis (at [REDACTED]) and characterization at the foundry. We will make use of atomic layer deposition facilities for surface passivation and protection.
<b>NCEM:</b> (support)	We will use NCEM for advanced TEM imaging of heteroepitaxial GaAs structures and oxide passivated III-V interfaces. This will be complementary to the Foundry facilities in this area.

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## Proposal Description

### Significance and Impact

Photovoltaics with higher efficiency (30-40%) and lower cost ( $<0.5\$/W_p$ ) are needed to drive the transition from fossil fuel-based economies to renewable energy-based economies. GaAs is a potential candidate for use in high-efficiency low-cost photovoltaics as well as advanced water-splitting devices. GaAs is used to make the best single-junction photovoltaics known, with recent AM1.5G  $\sim 28.8\%$  demonstrated, and tandems based on GaAsP and Si could theoretically attain efficiencies  $\sim 40\%$ . The commercial implementation of GaAs photovoltaics for non-concentrated one-sun applications, however, is currently prevented by the high cost of (1) metal-organic chemical vapor deposition (MOCVD), a batch vacuum-pressure deposition process which employs expensive, toxic and pyrophoric gas-phase precursors that are used with relatively low efficiencies (at best  $\sim 40\%$ ) and (2) epitaxial GaAs growth substrates. Industry is working to lower the cost of MOCVD and productionize epitaxial lift-off (ELO) techniques to reuse substrate wafers. It is unclear if this approach can meet the  $0.50\ \$/W_p$  SunShot module cost target because of the complexity of ELO, the precursor costs, and the capital expense of MOCVD. Our goal is to develop low-cost GaAs deposition technologies that yield high performance material on Si or foil substrates and significantly reduce the costs of GaAs and related III-V PV and solar water splitting devices.

We recently built a GaAs vapor-transport (VT) reactor that deposits GaAs thin films at ambient pressure using pressed GaAs powder as the sole precursor and dilute water vapor as the transport agent. We found that the GaAs films can be doped by adding dopant powders to the GaAs sources, and have now shown that GaAs films grown at  $\sim 0.5\text{ mm min}^{-1}$  possess diffusion lengths ( $L_D$ ) of  $\sim 3\text{ mm}$  for n-GaAs,  $\sim 9\text{ mm}$  for p-GaAs, and mobilities equivalent to MOCVD-grown GaAs. In addition, the GaAs powders which are used as source material can be relatively inexpensive, ( $\sim \$500/\text{kg}$ ), leading to conservative estimates for raw materials costs below  $\$0.05/W_p$  even for a film  $\sim 4\text{ mm}$  thick. These preliminary results motivate aggressive efforts to develop VT GaAs as a viable alternative for the scalable deposition of high-efficiency III-V's for terrestrial one-sun PV to meet the  $0.50\ \$/W_p$  SunShot module target. These materials may also find use in photoelectrochemical devices e.g. as water-splitting photoelectrodes.

### Project Plan

In the coming year our objectives are to (1) increase the efficiency of our GaAs pn homojunctions (2) develop close-spaced vapor transport (CSV) deposition routes to  $\text{GaAs}_x\text{P}_{1-x}$ , which will find use as window layers in GaAs cells or as absorber layers in tandems on Si, (3) continue nanopatterning defect-mitigation efforts towards growing III-V's on Si wafers thereby enabling the design/fabrication of low-cost tandem III-V on Si PVs with  $\eta > 30\%$  that leverage cost reductions in Si PV technology, and (4) investigate passivation of III-V and Si surfaces via atomic layer deposition (ALD) for aqueous photoelectrochemical applications.

We will improve the open-circuit voltage and quantum efficiency of our GaAs pn junctions by growing both the n-type emitters and p-type absorbers via CSV at [REDACTED]. We will measure the spectral response and current-voltage (J-E) response of the devices at [REDACTED]. The minority carrier lifetime of the absorber layers will be measured at LBNL using two-photon time-resolved photoluminescence. The carrier lifetime information will be used to improve our simulations at [REDACTED] so that we can better predict device performance and improve our CSV processes.

The foundry will provide tools and expertise needed to identify and quantify crystalline defects in our pn junctions and heteroepitaxial/epitaxial films. We will perform cathodoluminescence of planar samples and perform transmission electron microscopy (TEM) on cross-sectioned samples to measure threading dislocation density (TDD). Comparing TDD as a function of growth parameters will help us to optimize our growth procedure and achieve high efficiency  $\text{GaAs}_x\text{P}_{1-x}$ /GaAs pn photovoltaics and III-V/Si tandem photovoltaics. Comparing this information with the PEC data measured at [REDACTED] will give a more complete understanding of our material and allow us to further improve the materials growth.

Patterning substrates (Si and GaAs) for selected area epitaxy (SAE) will be done at LBNL using nanoimprint lithography. Patterning by nanoimprint lithography will allow SAE (done at [REDACTED]) of non-lattice matched materials while maintaining low TDD. We will continue using photolithography at the [REDACTED] as a proof-of-concept to explore and screen new patterns and geometries for SAE.

Thin layers of metal oxides will be deposited on GaAs samples at LBNL via atomic layer deposition (ALD). The oxide layers will be designed to enhance surface passivation and/or charge transport properties. These structures will be made into electrodes and their semiconductor/oxide interfaces will be probed in electrochemical cells at [REDACTED]. We will explore the effects of oxygen and hydrogen evolution catalysts on the semiconductor/oxide/liquid junctions.

## Molecular Foundry Utilization Timeline

We anticipate visiting the molecular foundry approximately once every 2-3 months during the next year. Each visit will last ~1 week. Funding for this visits are budgeted in our current DOS SunShot award.

Timeline:

- (1) Spring 2014 : Continue defect and lifetime measurements on p, n, and pn CSVT GaAs grown at the [REDACTED]
- (2) Early Summer 2014: Nanolithographic patterning and heteroepitaxial growth / heteroepitaxial growth characterization
- (3) Summer/Fall 2014: Start ALD surface protection/passivation studies
- (4) Winter 2014: Continue advanced characterization of materials and interfaces fabricated via [REDACTED]-Foundry collaboration.

## Relevant Experience

student name

[REDACTED] has conducted a great variety of experiments and measurements dealing with semiconductor-solution interfaces and materials chemistry. He has worked to develop a set of photoelectrochemical tools used to obtain information such as doping type and density, quantum efficiency, and minority carrier diffusion length. He designed and built the CSVT reactor, developed the GaAs deposition procedures used to make films with long diffusion lengths and mobilities, and proposed doping CSVT films by addition of dopant powders, which has enabled fabrication by CSVT of p- and n-GaAs with a wide range of possible dopant densities.

student name

[REDACTED] has a semiconductor physics background and is experienced with simulations and calculations relevant to solar cells. He developed the procedures used to make thin (<50 nm) pinhole-free GaAs emitters by CSVT and developed the procedures used at [REDACTED] to engineer GaAs thin films into solid-state PV devices with  $V_{OC} > 900$  mV. He has experience conducting drive level capacitance measurements which he uses to measure defect energy levels in GaAs homojunctions. He also wrote the software used to control and automate the CSVT.

student name

[REDACTED] has experience with both photoelectrochemistry from her summer internships at NREL and the design and synthesis of arrays of nanostructures by CSVT. She has also designed a variety of photolithography masks using CAD programs which have led to the deposition of cm-scale arrays of GaAs nanostructures via CSVT. She currently leads the [REDACTED]'s effort to create tertiary III-V films on GaAs using CSVT in order to use as window layers on epitaxial pn junction devices.

professor name

Asst. Prof. [REDACTED] is the project leader and has broad experience in semiconductor materials, solar energy conversion technologies, and electrochemistry (45 publications, incl. Science, Nature Mat. PRL, PNAS, JACS, etc., >3000 citations). He and his team are currently collaborating with Dr. Shaul Aloni at the Molecular Foundry, funded by a SunShot Bridge Award to support this work (450k + 45k match, 11/12 ? 11/15). Additional grants in collaboration with Dr. Aloni leveraging the work on GaAs and for photoelectrochemical applications as well as for next-generation passivated contacts have been submitted to DOE and NSF.

## Need for the Molecular Foundry

In order to improve the performance of our GaAs pn junctions we require a better understanding of the present limiting factors. In particular the bulk recombination lifetime is an important factor which dictates device performance. Due to the high surface recombination velocity of GaAs, surface-sensitive techniques such as time resolved photoluminescence cannot be used to determine the bulk minority carrier lifetime in GaAs. However, the Foundry's unique two photon time-resolved photoluminescence measurement will enable us to measure a bulk lifetime. After we know the lifetime we will be able to conduct more accurate modeling which will yield insights for the design of better devices.

We also propose to study the GaAs/metal oxide/H<sub>2</sub>O interface, which is fundamentally important for photoelectrochemical applications such as water splitting. Although GaAs itself is oxidatively unstable in water, if it could be protected by a non-porous metal oxide capping layer (one which was oxidatively stable in water), we could make use of the excellent optoelectronic properties of GaAs even in aqueous environments. Previous attempts to make electrodes of this structure were unsuccessful as the spin-cast metal oxide films had pinholes, which resulted in corrosion of the GaAs. In order to produce pinhole-free layers of metal oxide we propose using the ALD system at the Foundry and tune the composition to control charge transport. In addition, the imaging facilities available at the foundry will allow us to quickly evaluate the structure and properties of the ALD layers prior to our photoelectrochemical investigations at the [REDACTED]. We have also found the broad general expertise of Dr. Aloni and other Foundry staff and users to be a critical resource for our research. This is especially important, given the relatively small size of the [REDACTED] chemistry department and the lack of an engineering school at the [REDACTED].